

SI.No	Topics	Field
PSVLS 1	New Adaptive Weight Algorithm For Salt & Pepper Noise Removal (2011C)	IEEE 2011 (Low Power Design, Image Processing, System Generator, Signal Processing)
PSVLS 2	Removal Of High Density Salt & Pepper Noise Through Modified Decision Based Un-Symmetric Trimmed Median Filter	
PSVLS 3	Operation Improvement Of Indoor Robot By Gesture Recognition	
PSVLS 4	Adiabatic Technique For Energy Efficient Logic Circuits Design	
PSVLS 5	Enhancing Efficiency In SRAM Arrays Through Recovery Boosting	
PSVLS 6	Design And FPGA Implementation Of Modified Distributive Arithmetic Based DWT – IDWT Processor For Image Compression	
PSVLS 7	Enhancing NBTI Recovery In SRAM Arrays Through Recovery Boosting	
PSVLS 8	Optimization Of Processor Architecture For Image Edge Detection Filter	
PSVLS 9	Design And Analysis Of Two Low-Power SRAM Cell Structures	
PSVLS 10	A Novel Column-Decoupled 8T Cell For Low-Power Differential And Domino-Based SRAM Design	
PSVLS 11	CMOS Full-Adders For Energy-Efficient Arithmetic Applications	
PSVLS 12	Pipelined Architecture For FPGA Implementation Of Lifting-Based DWT	
PSVLS 13	Parallel Architecture For Hierarchical Optical Flow Estimation Based On FPGA	
PSVLS 14	A VLSI Architecture Of SVC Encoder For Mobile System	
PSVLS 15	Variability Resilient Low-Power 7T-SRAM Design For Nano - Scaled Technologies (2010C)	IEEE 2010 (Image Processing, System Generator, Signal Processing)
PSVLS 16	Design And Implement Of The Embedded Elevator Monitor System Based On Wireless Communication	
PSVLS 17	A real time implementation of Finger- Robot interaction using FPGA	
PSVLS 18	Power Estimation Of Embedded Multiplier Blocks In FPGAs	
PSVLS 19	Flexible Hardware Architecture Of Hierarchical K-Means Clustering For Large Cluster Number	
PSVLS 20	Keyless Car Entry Through Face Recognition Using FPGA	
PSVLS 21	An FPGA-Based Architecture For Linear And Morphological Image Filtering	
PSVLS 22	Image Edge Detection Based On FPGA	
PSVLS 23	Ground Bounce Noise Reduction Of Low Leakage 1-Bit Nano - CMOS Based Full Adder Cells For Mobile Applications	IEEE 2011
PSVLS 24	Design Of A Low Power Flip-Flop Using CMOS Deep Submicron Technology	
PSVLS 25	Low-Power And Area-Efficient Carry Select Adder	
PSVLS 26	A Pipeline VLSI Architecture For High-Speed Computation Of The 1-D Discrete Wavelet Transform	
PSVLS 27	FPGA Based Inexpensive Automobile Refuge System	
PSVLS 28	SIM Card Based Smart Banking Using FPGA	

PSVLS 29	Reconfigurable Hardware For Median Filtering For Image Processing Applications	IEEE 2011 (Low Power Design, Image Processing, System Generator, Signal Processing)
PSVLS 30	Design Of FFT Processor Based On FPGA	
PSVLS 31	A Color Image Segmentation Based On Region Growing	
PSVLS 32	Message Encoding In Images Using Lifting Schemes	
PSVLS 33	Dual Stack Method: A Novel Approach To Low Leakage And Speed Power Product VLSI Design	
PSVLS 34	Standby Leakage Power Reduction Technique For Nano - scale CMOS VLSI Systems	
PSVLS 35	Implementation Of Convolutional Encoder And Viterbi Decoder Using VHDL	
PSVLS 36	An FPGA Implementation Of The Time Domain Deadbeat Algorithm For Control Applications	
PSVLS 37	A New VLSI Architecture Of Parallel Multiplier-Accumulator Based On Radix-2 Modified Booth Algorithm	
PSVLS 38	A High Performance Binary To BCD Converter For Decimal Multiplication	
PSVLS 39	A Wide-Range All-Digital Delay-Locked Loop In 65nm CMOS Technology	
PSVLS 40	Motion Human Detection Based On Background Subtraction	
PSVLS 41	System Level Simulation Guided Approach To Improve The Efficacy Of Clock-Gating	
PSVLS 42	Design And Sensitivity Analysis Of A New Current-Mode Sense Amplifier For Low-Power SRAM	
PSVLS 43	An Enhanced Railway Transport System Using FPGA Through GPS & GSM	
PSVLS 44	Design Of Low-Power High-Speed Truncation-Error-Tolerant Adder And Its Application In Digital Signal Processing	
PSVLS 45	Adaptive 2-D Wavelet Transform Based On The Lifting Scheme With Preserved Vanishing Moments	
PSVLS 46	System Level Simulation Guided Approach To Improve The Efficiency Of Clock-Gating	
PSVLS 47	An Integrated Library Management System For Book Search And Placement Tasks	
PSVLS 48	Energy-Efficient Design Methodologies: High-Performance VLSI Adders	
PSVLS 49	FPGA-Based Implementation Of A Low Cost And Area Real-Time Motion Detection	IEEE 2011 (Low Power Design, Image Processing)
PSVLS 50	Design And Implementation Of Different Multipliers Using VHDL	
PSVLS 51	Hellfire: A Design Framework For Critical Embedded Systems' Applications	
PSVLS 52	FPGA-Based GPS Application System Design	
PSVLS 53	Performance Evaluation Of DES And Blowfish Algorithms	
PSVLS 54	A New And Efficient Algorithm For The Removal Of High Density Salt And Pepper Noise In Images And Videos	
PSVLS 55	Flexible Hardware Architecture Of Hierarchical K-Means Clustering For Large Cluster Number	
PSVLS 56	GPS-GSM Based Bus Stop Automation	

PSVLS 57	Low-Power Leading-Zero Counting And Anticipation Logic For High-Speed Floating Point Units (Verilog)	
PSVLS 58	Comprehensive Analysis And Control Of Design Parameters For Power Gated Circuits	
PSVLS 59	Design & Implementation Of A Low Power Differential Amplifier	
PSVLS 60	VLSI Implementation Of WIMAX Convolutional Code Encoder And Decoder	
PSVLS 61	An Optimized Tag Sorting Circuit In WFQ Scheduler Based On Leading Zero Counting	
PSVLS 62	Removal Of Sign-Extension Circuitry From Booth's Algorithm Multiplier-Accumulators	
PSVLS 63	Design Optimization Of FPGA Based Viterbi Decoder	
PSVLS 64	A Novel Cost-Effective Combine Generation And Cross-Talk Mitigation In Optical OFDM Signal Using Optical IFFT Circuits	
PSVLS 65	Transistor Count Optimization Of Conventional CMOS Full Adder & Optimization Of Power And Delay Of New Implementation Of 18 Transistor 1-V, High Speed, Low Leakage CMOS	
PSVLS 66	A High Performance Reconfigurable Motion Estimation Hardware Architecture	
PSVLS 67	Image Coprocessor: A Real-Time Approach Towards Object Tracking	
PSVLS 68	Significance Of Tree Structures For Zero Tree-Based Wavelet Video CODECS	
PSVLS 69	HW/SW Co-Simulation Platforms For VLSI Design	
PSVLS 70	A New Digital Watermarking Scheme Based On Text	
PSVLS 71	VLSI Architectures Of Perceptual Based Video Watermarking For Real-Time Copyright Protection	
PSVLS 72	Real-Time Invariant Textural Object Recognition With FPGAs	
PSVLS 73	Throughput Efficient Parallel Implementation Of SPIHT Algorithm	
PSVLS 74	FPGA Based Remote Integrated Security System Based WAP	
PSVLS 75	High-Speed FPGA Implementation For DWT Of Lifting Scheme	
PSVLS 76	Dynamic Power Analysis For Custom Designs	
PSVLS 77	Design And Implementation Of Mobile Based Electrical Appliances Control For Industrial Automation	
PSVLS 78	On Line Wavelets Transform On A Xilinx FPGA Circuit To Medical Images Compression	
PSVLS 79	Design Of Video Compression System Based On DSP-FPGA	
PSVLS 80	A Measurement System For The Performance Assessment Of Car-Integrated GSM Mobile Communications Systems	
PSVLS 81	A Design Of Bi-Verification Vehicle Access Intelligent Control System Based On RFID	
PSVLS 82	Full Coverage Manufacturing Testing For SRAM-Based FPGA	
PSVLS 83	High Speed VLSI Implementation Of A Finite Field Multiplier Using Redundant Representation	
PSVLS 84	Implementation Of A Hardware Functional Verification System Using System C Infrastructure	

PSVLS 85	Design And Development Of Activation And Monitoring Of Home Automation System Via SMS Through Microcontroller	IEEE 2011 (Low Power Design, Image Processing)
PSVLS 86	Design Of Reconfigurable LED Illumination Control System Based On FPGA	
PSVLS 87	Improved Method To Increase AES System Speed	
PSVLS 88	Design And Implementation Of Mobile Based Electrical Appliances Control For Industrial Automation	
PSVLS 89	Hand Gesture Recognition System Based On Associative Processors Real Time	
PSVLS 90	Experiences Using The Xilinx Micro Blaze Soft Core Processor And μ CLinux In Computer Engineering Capstone Senior Design Projects.	IEEE 2009 (Communication, Power Analysis)
PSVLS 91	Mean-Square Performance Of Selective Partial Update Sub-Band Adaptive Filters	
PSVLS 92	A Framework Of Transaction-Based HW/SW Co-Simulation For IC Verification	
PSVLS 93	Research On Image Median Filtering Algorithm And Its FPGA Implementation	
PSVLS 94	On Line Wavelets Transform On A Xilinx FPGA Circuit To Medical Images Compression	
PSVLS 95	Medical Image Fusion Based On An Improved Wavelet Coefficient Contrast	
PSVLS 96	Embedded A Low Area 32-Bit AES For Image Encryption/Decryption Application	
PSVLS 97	Broadband Receiver Design On FPGA	
PSVLS 98	Low Power And Area Efficient Image Segmentation VLSI Architecture Using 2-Dimensional Pixel-Block Scanning	
PSVLS 99	Quadrature Phase Shift Keying Modulator & Demodulator For Wireless Modem	
PSVLS 100	Low-Power Clocked-Pseudo-NMOS Flip-Flop For Level Conversion In Dual Supply Systems	
PSVLS 101	A Low-Power Delay Buffer Using Gated Driver Tree	
PSVLS 102	A Dynamically Reconfigurable Arithmetic Circuit For Complex Number And Double Precision Number	
PSVLS 103	An Efficient Hardware Architecture For Multimedia Encryption And Authentication Using The Discrete Wavelet Transform	IEEE 2009
PSVLS 104	Transaction Level Modeling For Early Verification On Embedded System Design	
PSVLS 105	A Low Overhead Fault Detection And Recovery Method For The Faults In Clock Generators	
PSVLS 106	A Framework Of Transaction-Based HW/SW Co-Simulation For IC Verification	
PSVLS 107	A HW/SW Co-Verification Technique For Field Programmable Gate Array (FPGA) Test	
PSVLS 108	High Throughput One Dimensional Median And Weighted Median Filters On FPGA	
PSVLS 109	Designing Of VGA Character String Display Module Based On FPGA	
PSVLS 110	Implementation Of Tsunami Alert System Using FPGA	
PSVLS 111	Finger Print Based Authentication and Controlling System of Devices using FPGA	
PSVLS 112	An efficient FPGA implementation of secure cryptographic technique using Wireless Body Area Network.	
PSVLS 113	Pulse Propagation Along Single-Wire Electric Fences(2008T)	

PSVLS 114	Multi-sensory system for obstacle detection on railways	IEEE 2009
PSVLS 115	Pulse Propagation Along Single-Wire Electric Fences	
PSVLS 116	FPGA based System for Enhancing Medication Safety and Healthcare for Inpatients Using RFID	
PSVLS 117	An Optimized RFID-Based Academic Library	
PSVLS 118	Real-time Binary Shape Matching System Based on FPGA	
PSVLS 119	An RFID Based Solution for Real-Time Patient Surveillance and data Processing Bio-Metric System using FPGA	